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13. ABSTRACT (Maximum 200 words)

Substantial progress has been made in a number of areas to improve the reproducibility and quality of AlN films produced under the program. To date, more than twenty films have been prepared under UHV conditions. In the course of the work, a number of important conditions which affact film growth have been identified. These Include:

-substrate cleaning - it was shown that simple heating is not effective in removing all predeposition surface carbon deposits. A Multiple etch procedure was developed which results in carbon free surfaces
-AlN film formation- the effects of substrate temperature were explored. No stron correlation was found between the substrate temperature and density of interface states
-Al capping - a technique was developed to protect the AlN films from oxidation by the depostion of a layer of Al on the AlN following growth. This precedure produced the best C-V results to date- hysteresis - inversion was demonstrated on AlN films for applied voltages between 1.5 and 5 volts. The indications are that

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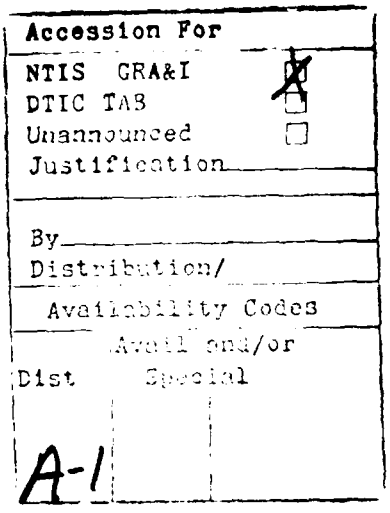
residual hysteresis in not due to interface states, a most encouraging sign.



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AlN INSULATOR FOR III-V MIS APPLICATIONS

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1.0 INTRODUCTION

The development of a generally useful MIS technology for III-V semiconductors could be important for a number of digital and analog circuit applications. To be generally useful, the insulator in the MIS structure should have a high resistivity and a low density of traps; in addition, the insulator/III-V interface must have a low interface state density. A large majority of III-V MIS studies have utilized native oxides as insulating layers in an attempt to mimic the very successful MIS characteristics of the Si/SiO_2 interface. However, the chemical nature of native oxides which form on III-V semiconductors is more complex than SiO_2, and it is frequently observed that these oxides are poor insulators, have substantial trap concentrations, and the oxide/III-V interface state densities are unacceptably large. These unfavorable properties cause undesirable hysteresis in electrical characteristics and make it difficult to alter substantially the semiconductor interface potential. Thus, high speed integrated circuit and opto-electronic applications which could employ a III-V technology are not currently feasible.

Several III-V semiconductors have material properties which would be superior to Si in selected device applications. The high electron mobility and peak saturated electron velocity of GaAs, for example, make GaAs of technological importance for high speed and high frequency devices. Complex high speed digital integrated circuits have been fabricated with normally-on depletion mode GaAs MESFET technology.[1,2] If a normally-off enhancement mode GaAs FET technology could be developed, it would have the advantage of lower power consumption and simpler circuit design. The use of an insulated gate as opposed to a Schottky barrier gate in an enhancement mode FET application would permit larger logic swings and greater flexibility in device design. A MISFET avoids the necessity of critically controlling the pinch-off voltage as is required for successful operation of a forward biased enhancement mode MESFET device. Although GaAs MISFET devices have been successfully fabricated for use at microwave frequencies, low frequency operation is presently limited by inability to minimize sufficiently interface state densities.

If a useful GaAs MIS technology can be developed, the multigigabit data rate enhancement mode FET should be an attractive device application. This device would have a wide dynamic range because the positive gate voltage utilized to produce the inverted channel in the normally-off device would be limited only by the breakdown voltage of the gate insulator. Thus, a direct coupled logic design, which does not require level shifting as in the normally-on depletion mode MESFET technology, should be possible. The simpler circuit design which involves only a single power supply and has lower power dissipation should produce a more compact device structure.

This proposal is for a two year extension of the current program whose aim is to develop AlN as a useful insulator for III-V MIS applications. The rationale for investigating the use of AlN as an insulator on III-V semiconductors is reviewed in Section 2. Recent progress of the program is discussed in Section 3; this includes refinements of the reactive MBE AlN deposition apparatus (Sec. 3.1), investigation of the AlN deposition process (Sec. 3.2), characterization of the AlN material properties (Sec. 3.3), measurement of the AlN film electrical properties (Sec. 3.4), and an outline of plans for the remainder of the current program (Sec. 3.5). The proposed technical program is discussed in Section 4. Several possible new process refinements are suggested in Section 4.1. Additional electrical measurements needed to characterize the resulting MIS structures are discussed in Section 4.2. The fabrication and testing of MISFET structures is outlined in Section 4.3. Additional related studies are suggested in Section 4.4 to investigate the possibility of introducing shallow donors into AlN and to characterize interfaces formed between AlN and selected III-V semiconductors other than GaAs. Sections 5 through 8 contain the Work Statement, a Facilities section, a Personnel section and References, respectively.

2.0 BACKGROUND

Most previous work on developing MIS for III-V applications has relied on using native oxides. For GaAs MIS, in particular, the basic oxidation techniques that have been tried include anodic, thermal, and various types of plasma oxidation; extensive literature references are available in Refs. 3-6. Studies of deposited oxides (and other materials) for MIS applications have also been reported. In most cases, when nonoxygen-containing deposited insulators have been studied, the GaAs substrate had several monolayers of native oxide present prior to insulator deposition. The presence of several monolayers of oxides may cause undesirably large interface state densities.

The most common oxides present on GaAs surfaces are Ga_2O_3 and As_2O_3. Several studies[7,8] have shown that As_2O_3 is unstable in the presence of GaAs and that the reaction $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As$ readily occurs at the native oxide/GaAs interface. The elemental As produced in this reaction may be a major source of interface states and affect GaAs MIS characteristics. Similar oxide instabilities may be common for many III-V semiconductors.

In recent years, strong evidence in support of a defect model for Fermi level pinning at compound semiconductor interfaces has developed.[9-11] Although the atomic nature of the defects is not clear at present, and whether or not more than one characteristic defect is needed to account for the pinning positions observed on a particular III-V semiconductor is an undecided issue, there is reasonable concensus that the defects induce localized levels in the III-V semiconductor bandgap which can then pin the Fermi level at the energy of the defect level. For GaAs it is observed that deposition of several metals onto the surface or exposure of the GaAs surface to oxygen causes the Fermi level to be pinned near mid-gap. The large densities of interface states which are frequently observed in GaAs MIS structures may be associated with the same defects which cause Fermi level pinning.

The minimization of intrinsic defects at III-V/insulator interfaces could be a key factor in the fabrication of generally useful III-V MIS devices. One possibility that has been explored is the use of a lattice-matched heterojunction to form the interface to GaAs. Members of the $Al_xGa_{1-x}As$ system have been studied for this purpose in which the insulator was formed by either introducing oxygen into the $Al_xGa_{1-x}As$ to make it semi-insulating[12] or by thermally oxidizing the $Al_xGa_{1-x}As$.[13] One main difficulty encountered in attempting to use $Al_xGa_{1-x}As$ as an MIS insulator is that the bandgap is too small to provide good insulating properties (the bandgap of AlAs is 2.2 eV).

It may not be necessary to use lattice-matched heterojunctions in order to form a low interface state density MIS structure on III-V semiconductors (the SiO_2/Si interface is not lattice-matched). From consideration of the defect model of Fermi level pinning briefly mentioned above, it may be more important to choose an insulating material which will minimize defect related interface levels. An obvious possibility is to utilize a wide bandgap III-V material. The isoelectronic nature of this material could minimize both characteristic defects (e.g., vacancies and antisites) and impurity induced interface states. Only a few III-V materials would be suitable candidates for use as insulators. If one rules out materials with bandgaps $\lesssim$ 3 eV and requires thermal stability of the material, only AlN and BN are promising candidates.

AlN, which has a bandgap of 6 eV, is easier to prepare than BN. It has been used as a successful capping material for GaAs ion implantation studies.[14] Both Al_{Ga} and N_{As} are electrically inactive in GaAs and AlN is stable in vacuo to high temperatures. AlN is also stable in air. The thermal expansion coefficients of AlN and GaAs are nearly identical, and as a consequence, strain at the GaAs/AlN interface associated with thermal cycling is minimal and good adhesion is normally obtained. For these reasons, the main goal of this program is to explore the concept of using AlN as the insulator for III-V MIS applications.

3.0 RECENT PROGRESS

In this section, we discuss recent progress directly related to development of an AlN/GaAs MIS technology. This progress includes refinements in the reactive MBE AlN deposition apparatus (Sec. 3.1), development of the AlN deposition process (Sec. 3.2), and characterization of AlN films and MIS studies (Secs. 3.3 and 3.4). Section 3.5 briefly outlines plans for the remainder of the current program.

3.1 Apparatus Improvements

Immediately preceding the initiation of this program, several substantial improvements were made to the reactive MBE AlN deposition apparatus with company support (at no cost to this program). Because these improvements greatly enhance our ability to fabricate AlN/GaAs interfaces, they are briefly mentioned here.

A photograph of the AlN deposition apparatus is shown in Fig. 1. In order to increase sample throughput and maintain vacuum integrity, a load lock was added to the system. Before the addition of this load lock, the cycle time of the system was about 1.5 days per sample; the present cycle time is $\approx$ 2 hours. In addition to providing a more efficient means to optimize the deposition process, the load lock improves our ability to decrease background impurity levels.

To facilitate temperature control of the substrate, a Varian MBE 2" heated substrate station was installed in the system. Temperature control of the GaAs substrate is an important factor in the AlN deposition process which is discussed in Section 3.2.2. This heated substrate station considerably improves our ability to reliably control and set the substrate temperature.

An effusion cell has been constructed for the NH_3 source. By monitoring the NH_3 pressure in the cell, it is possible to control the NH_3 flux at the sample surface. A MBE Al source has been added to the system. This source makes it possible to obtain a controlled and stable Al flux. In

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Fig. 1 AlN deposition apparatus.

combination with the load lock mentioned above, the Al source contamination problems have been reduced substantially.

In addition, an Auger electron analysis system has been added to the apparatus which makes it possible to monitor the GaAs surface composition prior to deposition and the AlN composition resulting from the deposition.

3.2 AlN Preparation

As described in the preceding section, improvements in the apparatus have enabled us to obtain better control over the deposition process and to perform in situ characterization of AlN films by using Auger electron spectroscopy. Substantial progress has been made in a number of areas to improve the reproducibility and quality of AlN films produced under the current program. To date, more than twenty films have been prepared under UHV conditions by using the improved apparatus. In the course of the current program, we have identified a number of important conditions which affect film growth. Details of these studies are presented in the following sections.

3.2.1 Substrate Cleaning

Films have been grown on GaAs (100) oriented substrates which have been cleaned by heating the substrate to temperatures in excess of 600°C. Auger electron analysis of surfaces initially prepared with this method indicated that residual carbon on the substrate was not removed by the heat treatment. In addition, excess carbon from the Auger electron gun was deposited on the substrate during the analysis. Even though such contamination was typically less than a monolayer, the effects of such coverage on the properties of the film were substantial.

SEM micrographs (Fig. 2) show a considerable difference in morphology for regions of a substrate with carbon contamination. This change is visible optically as variations in color of the AlN film across the substrate following deposition, which indicates a change in the optical thickness of the film (film color is due to interference fringes and represents the optical film thickness).

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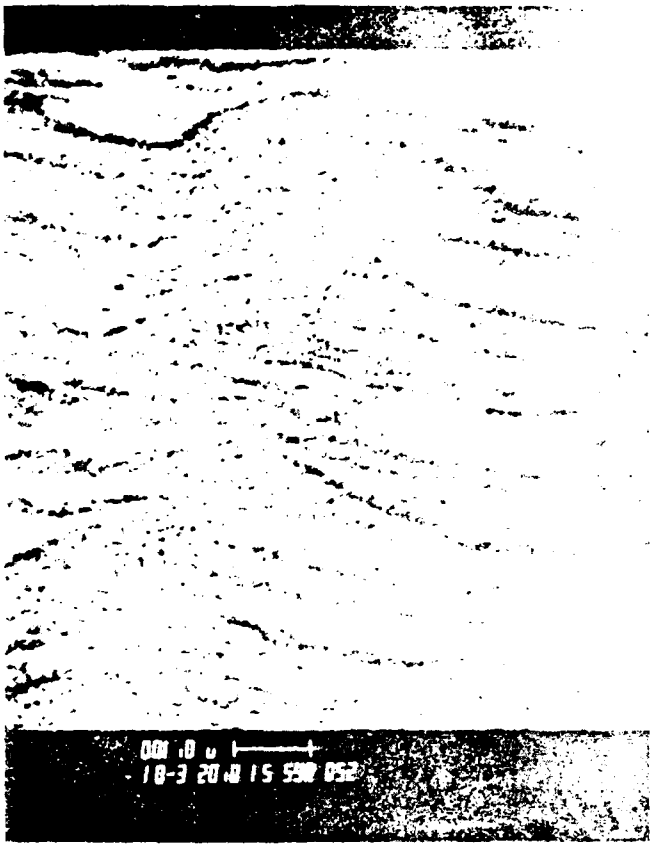

Fig. 2 SEM photograph of AlN/GaAs film with surface initially contaminated by carbon.

A procedure has been developed for eliminating excess carbon from the surface of the GaAs. As a result, we can obtain GaAs surfaces which are atomically clean as observable by using Auger analysis. This procedure consists of 1) degreasing the GaAs using conventional solvents, 2) etching the GaAs with a $NH_4OH:H_2O_2:2H_2O$ solution, and 3) attaching the GaAs substrate to a Mo substrate holder with high purity In. A final step consists of etching the GaAs with a 7:1:1 solution of $H_2O:H_2O_2:NH_4OH$ while spinning the substrate, followed with a rinse of 18 Megohm-cm water and finally spin-drying. The GaAs substrate prepared in this fashion is carbon-free and suitable for heat cleaning.

The thermal stability of the GaAs surface was investigated by heating several samples under UHV at various temperatures. Half of each sample was covered with Si_xN to prevent evaporation from this part of the surface. After heating the sample, the Si_xN was removed and the height of each area was compared. These results indicated that GaAs evaporation was negligible at temperatures less than 675°C. At this temperature, roughly 100Å of GaAs evaporated in 30 minutes, assuming congruent evaporation. No gross deterioration was observed, i.e., the surface remained specular. Therefore, we can conclude that macroscopic degradation of the substrate is negligible at lower temperatures.

3.2.2 AlN Film Formation - Temperature Dependence and Chemistry

We have made some preliminary studies of AlN film formation as a function of substrate temperature. Our results agree with those previously published for growth of AlN on Si. The ammonia flux necessary for stoichiometric film growth increases rapidly below 600°C. For practical conditions, such as growth rates ~ 100Å/min and NH_3 partial pressures < 10^{-3} Torr in the system, the temperature for stoichiometric growth must be greater than 550°C. The oxygen desorption temperature of GaAs (which is ≈ 600°C) is a convenient temperature for film deposition in that the substrate temperature need not be changed between substrate cleaning and film growth. As discussed

in Section 3.4.2, we have not found a strong correlation to date between the substrate temperature and density of interface states.

3.2.3 Al Capping

We have developed a technique for protecting the AlN layer from subsequent oxidation. As discussed in Section 3.3.4, a ≈ 10Å thick layer of oxide forms on the AlN surface upon exposure to air. Traps at the oxide-nitride interface may cause hysteresis in the MIS characteristic. To prevent this kind of trapping, a layer of Al was deposited on the AlN following growth. Such structures have given the "best" C-V characteristics observed to date.

3.2.4 In Contamination

The sample is attached to the substrate holder by wetting both the sample and substrate holder with molten In. During growth, we have discovered that excess In can catastrophically react with AlN to form an Al-In alloy and gaseous nitrogen. The In creeps over the sample surface during this reaction. Although the effect can be eliminated by using less In and a larger sample, the best solution may be to eliminate the In with a different sample holder configuration.

3.3 AlN Properties and Characterization

AlN films produced in the current program have been characterized by a number of techniques including Auger analysis, x-ray diffraction, SEM, XPS, far infrared transmission and Raman spectroscopy.

3.3.1 Auger Analysis

The addition of an Auger electron spectrometer to the growth apparatus has enabled us to characterize the purity of AlN films grown on GaAs in situ. A typical Auger electron spectrum of an AlN film immediately following growth is shown in Fig. 3. The predominant peaks in the spectrum

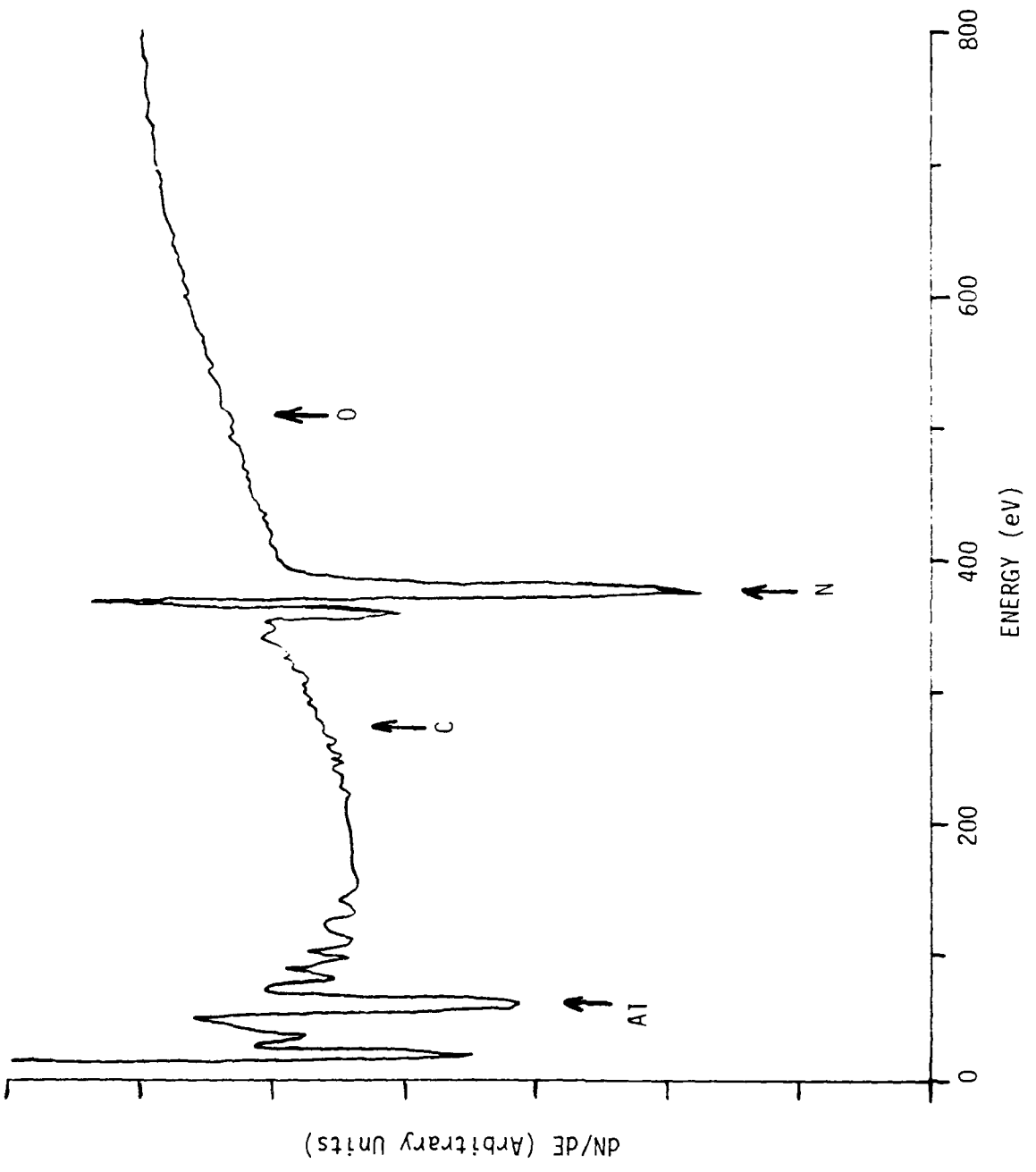

Fig. 3 In-situ Auger spectrum of AlN film grown on GaAs. Note the absence of oxygen and carbon in the spectrum.

are associated with Al at 57 eV and N at 381 eV. Oxygen and carbon are not detectable in the spectrum, which indicates that the films have good purity. For the spectrum shown in Fig. 3, we have estimated the composition to be stoichiometric AlN with [Al]/[N] = 0.94 ± 0.15. We can estimate the oxygen content to be less than 0.2% from the same spectrum.

Occasionally, we have observed the presence of Ga and As in the films, particularly for films grown at higher temperatures. We have not detected the presence of other elements in our films.

3.3.2 X-Ray Analysis

We photographed the CuKα x-ray diffraction powder pattern of an AlN film with a Gandolfi camera. The sample was approximately a square millimeter in size and had been removed from the substrate. The Gandolfi camera rotates this sample around two axes inclined 45° to one another to generate a series of random orientations as required to photograph the powder pattern. The photograph shown in Fig. 4 is a 72 hour exposure. This relatively long exposure time is required because of the relatively small mass of the thin sample. The pattern in Fig. 4 matches the published pattern[15] well. The pattern is that of the wurtzite type of crystal structure, which is hexagonal with space group $P6_3mc$. Lattice parameters measured from the photograph are a = 3.12 ± 0.01Å and c = 4.98 ± 0.01Å. These values agree with the published values within the indicated experimental error. The diffraction maxima in the photograph are rather broad; the $K\alpha_1$-$K\alpha_2$ doublet is not resolved. This line broadening is probably the result of strain or the effect of small crystallite size.

3.3.3 SEM Analysis

As indicated above, the films are composed of stoichiometric AlN which is probably polycrystalline. Scanning electron microscopy (Fig. 5) shows that the films grown with proper substrate preparation (see Sec. 3.2.1) have granular morphology with features approximately 1000Å across. It is possible that we are observing individual crystallites of AlN. Such an interpretation would be consistent with the x-ray results (see Sec. 3.3.2).

Fig. 4 Gandolfi x-ray photograph of AlN film.

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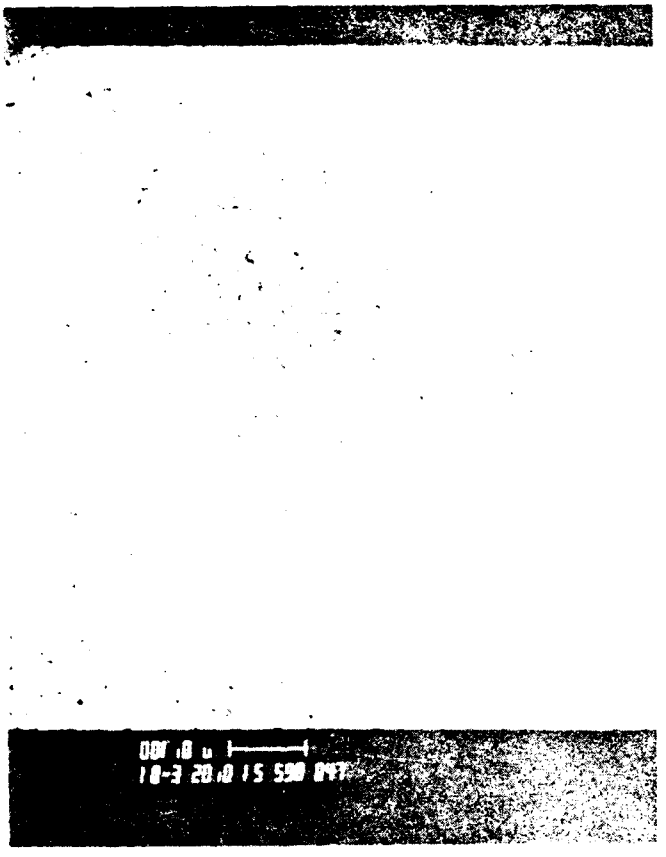


Fig. 5 SEM photograph of AlN/GaAs film showing granular morphology.

3.3.4 XPS Analysis

X-ray photoemission spectroscopy (XPS) was used to analyze the surface of a thick ($\approx 10^3$Å) AlN film grown on GaAs (100) in the reactive MBE deposition system (Sec. 3.1), and subsequently transferred in air into the XPS apparatus. A spectrum is shown in Fig. 6. The substantial O1s signal observed in this spectrum indicates that ≈ 10Å of the surface is oxidized by air exposure. Thus, as mentioned in Section 3.2.3, it may be important to cap the AlN with a metal before removing it from the MBE system to prevent traps from forming due to the presence of the thin oxidized AlN layer.

3.3.5 FIR and Raman Analysis

We have investigated the properties of the AlN films and the GaAs substrate with far infrared transmission (FIR) and Raman scattering spectra. Figure 7 shows a typical transmission spectrum of an AlN layer on a bulk GaAs substrate between 500 cm^{-1} and 1000 cm^{-1} (20 μ and 10 μ, respectively).

The GaAs substrate is relatively transparent in this spectral range, except for a two phonon peak at 520 cm^{-1}. The spectrum shows peaks at 610 cm^{-1}, 650 cm^{-1} and 671 cm^{-1}, corresponding to lattice TO phonons in AlN. These values compare with 610 cm^{-1}, 655 cm^{-1} and 667 cm^{-1} for results obtained on bulk AlN crystals.[16] These results support the Auger and x-ray analyses which indicate the films consist of stoichiometric polycrystalline AlN.

We have also looked at Raman spectra of the underlying GaAs substrate. Such spectra have previously been interpreted in terms of strain at the insulator/GaAs interface.[17] We observe the GaAs LO phonon mode at 291 cm^{-1} with a width of 7 cm^{-1}. This can be compared with a width of 5 cm^{-1} for a clean GaAs surface. We conclude that strain related broadening of the Raman line is minimal for the AlN deposited on GaAs by reactive deposition.

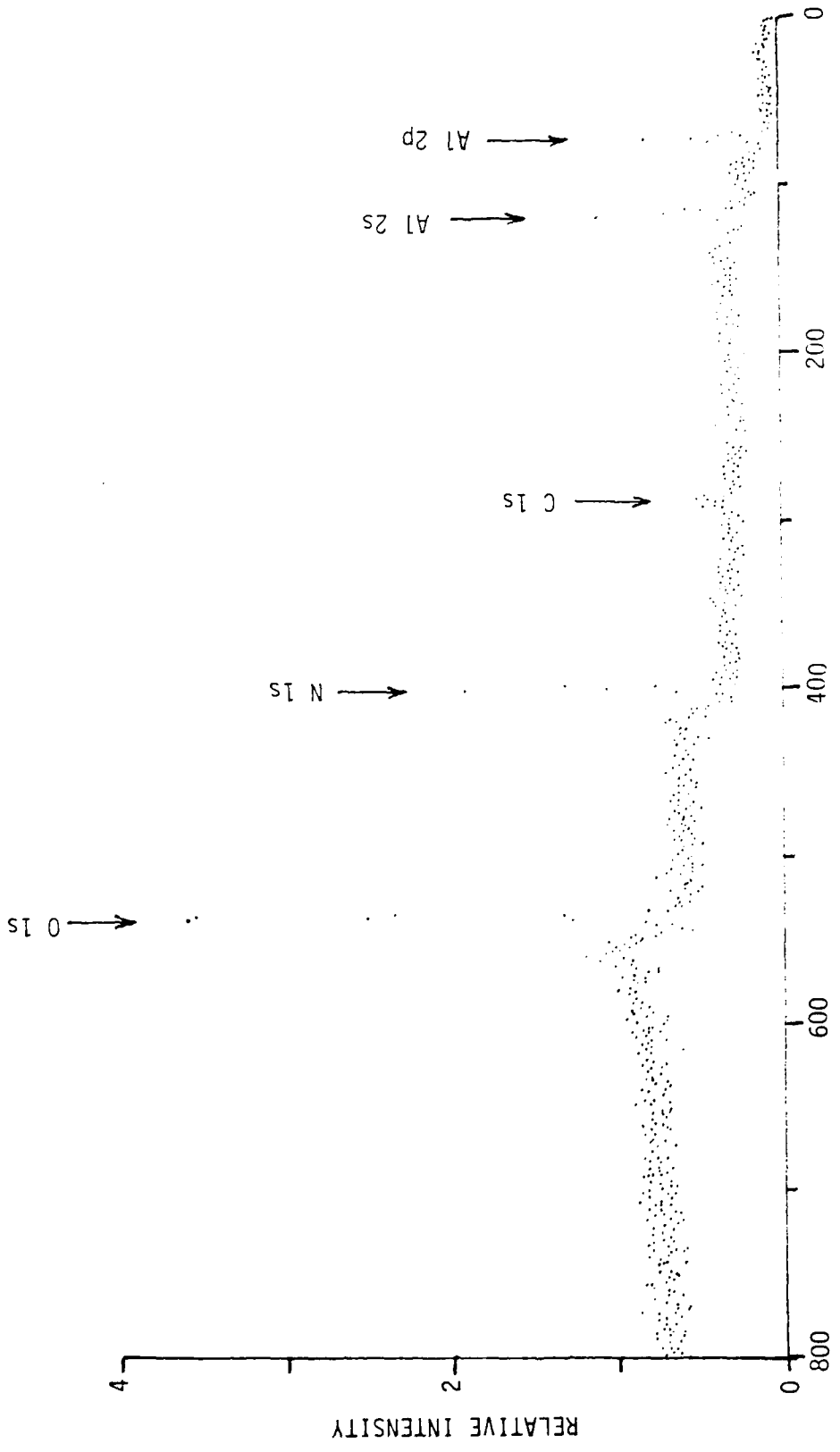


Fig. 6 XPS spectrum of AlN surface after several hours of air exposure.

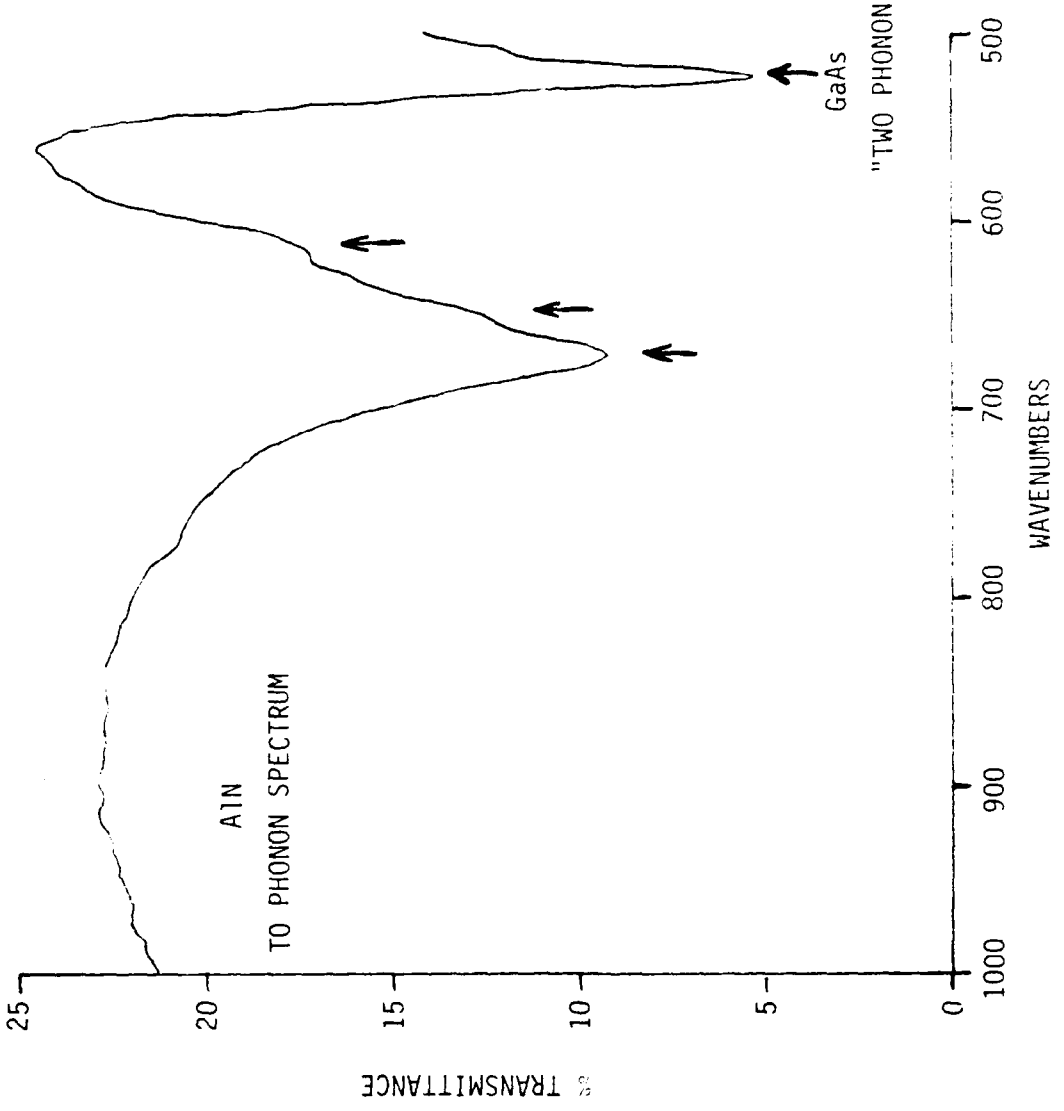


Fig. 7 Infrared absorption spectrum of AlN film grown on GaAs substrate which shows transverse optical modes (marked by arrows) associated with AlN.

3.4 Electrical Properties of the Films

In this section we analyze electrical and MIS properties of the AlN films grown on GaAs (100).

3.4.1 Frequency Dispersion

To determine the dielectric properties, variable frequency C-V measurements have been made for AlN films grown on degenerately doped GaAs substrates. The thickness of the films was determined optically and found to be inversely proportional to the capacitance as expected. The results of these measurements are shown in Fig. 8. At low frequencies, the dielectric constant of the insulator increases rapidly. The high frequency dielectric constant corresponds to a value of 8, close to that reported for bulk AlN. A number of explanations can account for this behavior; the most likely is that the dispersion results from conduction associated with trapping centers in the insulator.

3.4.2 Analysis of C-V Data

Variable frequency capacitance voltage measurements have been made on a number of samples and analyzed to obtain an effective interface charge density to be used as a figure of merit for the C-V results. For the purpose of simplification, this charge density is simply $Q = C_{ins} \Delta V_{FB}$, where Q is the density of interface charge, C_{ins} is the insulator capacitance per unit area, and ΔV_{FB} is the difference from the theoretical flatband voltage. The source if such charge can, in fact, be traps in the insulator or at the semiconductor interface.

For films grown to date, Q has ranged from values as high as $10^{13} cm^{-2}$ to values as low as $4 \times 10^{11} cm^{-2}$ in the "best" samples. The origin of fluctuations in Q has not been determined. We have not been able to correlate Q with either the sample deposition temperature or the Al/NH_3 flux ratio during growth.

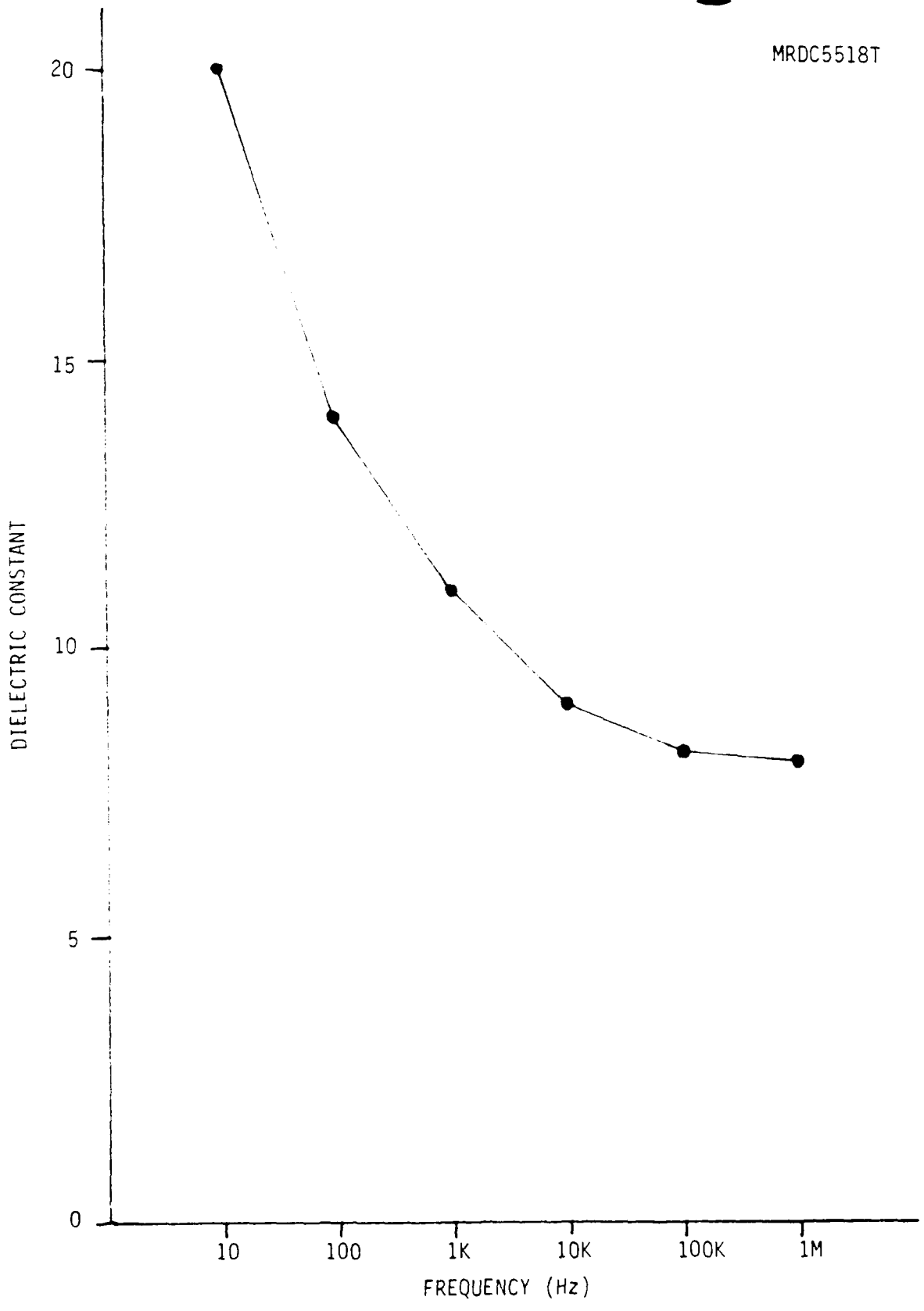


Fig. 8 Dispersion of dielectric constant for AlN film on n^+ GaAs substrate.

A theoretical fit to the "best" C-V curve obtained to date is shown in Fig. 9. The only parameters used to fit the curve are the insulator capacitance and substrate doping. A value of 35 pF was found to agree with the insulator capacitance obtained from the thickness of the layer and the area of the metal dot. The doping level is obtained from fitting the C-V curve in deep depletion. As can be seen from the fit, we appear to obtain inversion between 1.5 and 5 volts. Another encouraging aspect of these data is that the hysteresis occurs in a clockwise direction. If the hysteresis was associated with interface states, we would expect hysteresis in the opposite direction, indicating that the primary origin of the hysteresis is not due to interface states, but rather due to charge injection into the insulator or mobile ions. One possible origin of the hysteresis is due to contamination from residual water vapor and other oxygen-containing species in the vacuum system. A cryopump is to be added to the system to help reduce the amount of contamination from such sources. Another possibility is that a thin oxide layer formed following growth on the AlN upon exposure to air contributes to the hysteresis. Such effects are being studied by capping the AlN film with gate metallization in situ following growth as discussed in Section 3.2.3.

3.5 Plans for Remainder of Current Program

The primary activity anticipated during the remainder of the current program will involve systematically varying growth parameters to determine how to obtain our "best" C-V results for AlN/GaAs MIS structures routinely on a run-to-run basis and to optimize the process. For the present AlN growth process, these parameters involve growth temperature, Al/NH_3 flux ratio, growth rate, GaAs surface preparation, and possible effects of contaminants from source materials and the sample mounting procedure. A cryopump will be added to the reactive MBE system (at no cost to this program) in order to further minimize reactive background gases. Experiments will be conducted to determine if the thin oxidized AlN layer formed by air exposure prior to metallization has an effect on MIS characteristics.

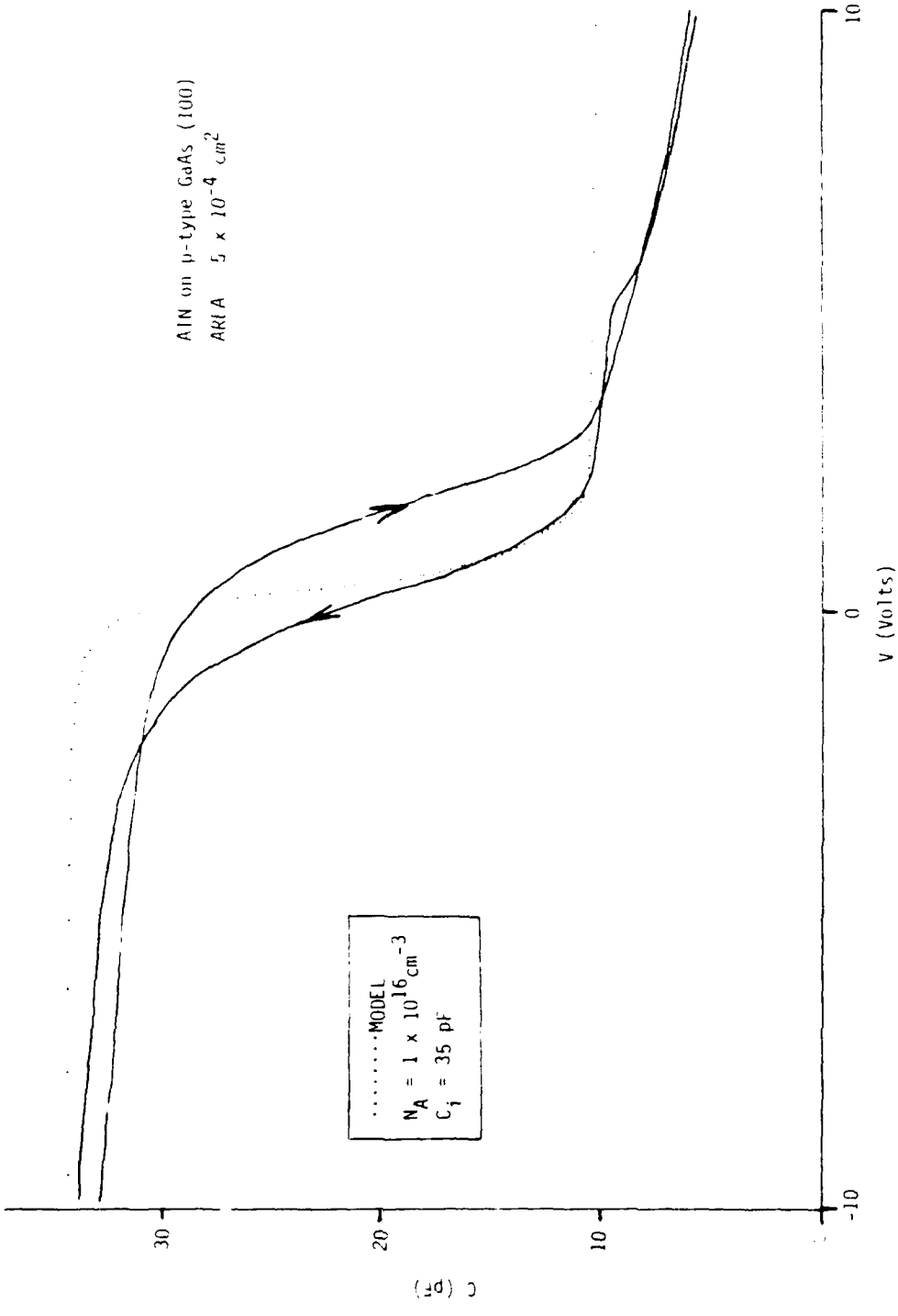


Fig. 9 C-V plot (1 MHz) for "best" MIS structure grown to date. The hysteresis is not consistent with charging of interface states but rather with charge injection or ion migration from the metal gate. A theoretical fit to the data is also shown.

4.0 TECHNICAL PROGRAM

In this section, we discuss a two year program which is proposed as an extension of the current program to develop AlN as an insulator for III-V MIS applications.

4.1 Process Refinement

Several possible new process variables are discussed in this section.

4.1.1 Addition of As Source to MBE System

We have plans to add an As_4 MBE source to the AlN deposition system. The addition of the As source will enable us to heat clean the GaAs surface at higher temperatures and to prevent deterioration of the GaAs surface. Since the interface state density may be associated with intrinsic defect formation caused by As loss from the surface during cleaning, the use of an As source may improve the interface quality and permit control of the interface state density. In addition, alteration of GaAs surface stoichiometry should be possible with the addition of the As source to the system.

By having an As source present on the AlN deposition system, it will be possible to cap samples with a protective layer of elemental As, which will permit easy transfer of samples between UHV systems for interface and compositional analysis. Elemental As can be removed from a sample surface by heating in UHV to $\approx$ 300°C; we have previously demonstrated this technique for $Al_xGa_{1-x}As$ sample transfer. It will be possible to grow very thin ($\approx$ 20Å) layers of AlN on GaAs substrates, cap them with As and transfer them into an XPS apparatus for analysis of the interface composition. In addition, such samples will permit an XPS measurement of the relative positions of the AlN and GaAs energy band edges at the interface. We have described this procedure for measuring band offsets several times in the literature (see, e.g., Ref.18). This band offset information will be useful to interpret the AlN doping studies which are described below in Section 4.4.2.

4.1.2 Substrate Material & Crystallographic Orientation

In the initial phase of this program, AlN layers have only been grown on GaAs substrates prepared by the horizontal Bridgman method with (100) orientation. The quality of this bulk substrate material is uncertain and may affect MIS properties. We propose to investigate bulk substrate material from other sources, including material grown by the liquid encapsulated Czochralski (LEC) technique from pyrolytic BN crucibles; this latter material is currently available from internal Rockwell International sources. Another material to be investigated is MBE grown GaAs which can be prepared with good reproducibility. In addition, this MBE grown material can be capped with As following growth to prevent atmospheric contamination during transfer into the AlN deposition apparatus.

Substrate orientation may also be an important parameter for growing AlN films. The orientation of the substrate will affect the crystallinity and morphology of the films a great deal. The films we have produced to date are most likely polycrystalline. Since single crystal or amorphous films would be preferable from the standpoint of eliminating grain boundaries, we feel that investigations of substrate orientation should have high priority.

4.1.3 Controlled Oxidation

It is possible that residual oxygen in the UHV vacuum system can have a substantial effect on the electrical properties of the AlN films. Such oxygen is normally present in the form of H_2O, CO and CO_2. We plan to test the effects of residual oxygen on the quality of our layers by intentionally adding controlled amounts of oxygen or oxygen-containing species into the vacuum system during, or prior to, film growth.

By selecting the time during growth at which oxygen is added, we can independently test effects on the AlN/GaAs interface, the bulk AlN film, and the metal/AlN interface. This should indicate the extent to which residual oxygen as a contaminant is a problem, and at what point during growth oxygen contamination is most critical.

4.2 MIS Measurements

Variable frequency C-V measurements will be used as the principle method of MIS characterization. Such measurements are fast and simple for the determination of interface properties, and have already been described in Section 3.4.2. I-V measurements will continue to be used to monitor insulator properties.

On selected samples, we plan to use DLTS (deep level transient spectroscopy) for more detailed investigations of interface state distributions. Such samples should have reasonably low interface state densities so that the sample can be driven into accumulation and deep depletion reliably.

The basic technique is an adaptation of DLTS as suggested by Lang;[19] DLTS is widely used to detect deep defect levels in bulk materials. To study interface states, a MIS structure is used. Consider such a structure with an n-type semiconductor. During a large forward bias voltage pulse, the device is driven into accumulation which fills the states at the interface with electrons. Following this pulse, the device is reverse-biased into deep depletion. The release of charge from the interface is measured by observing the corresponding change in capacitance of the device.

The DLTS signal is measured by taking the difference in capacitance at two times t_1 and t_2 after the transient. For an exponential transient, this gives a peak signal when

$$\tau = (t_2 - t_1)/\ell n\ (t_2/t_1) \quad , \tag{1}$$

where τ is the time constant of the transient. Also, the emission time constant is a strong function of temperature for a single state of given energy,

$$1/\tau = \sigma_n v_{th} N_c \exp(-E/kT) \quad , \tag{2}$$

where σ_n is the capture cross-section, v_{th} is the thermal velocity, N_c is the effective conduction band density of states, and E is the energy of the state

relative to the conduction band minimum. Because changing temperature results in a change of the emission time constant, one observes a peak in a plot of the DLTS signal vs temperature when Eq. (1) is satisfied.

By measuring several spectra with different t_2 and t_1, the variation of τ with temperature can be determined. By using Eq. (2), this information can be used to obtain the energy of the defect. If different defects occur, they produce separate peaks in the spectra, the height of the peak being related to the density of the defect.[19] It is possible to separate bulk from surface effects by varying the forward bias pulse so that the interface states are not charged. In this case, only a bulk spectrum is observed. Bulk states should only play a minor role for spectra taken on GaAs MIS devices. The concentration of deep levels in bulk GaAs is typically about $10^{15}cm^{-3}$. Thus, in a depletion layer ~ 1000Å wide, there are between 10^{10} and 10^{11} states cm^{-2}. However, the interface state density is generally much higher than this, about 10^{12} - 10^{13} states cm^{-2}.

There are two different methods for determining the density of interface states as a function of energy. In the first of these, the forward bias pulse is adjusted to drive the surface Fermi level to different values. The difference in charge released between two different values of the surface potential gives the interface state density.[20] This technique is not particularly useful for interface state analysis in GaAs for a number of reasons. First of all, the large frequency dispersion associated with interface states makes evaluation of the surface potential difficult. Secondly, it requires very long times at low temperatures to charge the interface states, since thermal equilibrium between the surface and the bulk is required for the analysis to be correct. Thirdly, local surface potential variations cause a loss in energy resolution.

A second method relies on the strong temperature dependence of the emission rate and is more appropriate for GaAs because it is not sensitive to dispersion and hysteresis effects.[21,22] For this method, we note that for a distribution of states $N_{ss}(E)$ with a capture cross-section $\sigma(E,T)$ the released charge is

$$\Delta Q = q \int_{-\infty}^{\infty} N_{ss}(E) \left[\exp(-t_1/\tau) - \exp(-t_2/\tau)\right] dE \quad . \tag{3}$$

For given values of t_1 and t_2, it can be shown[22] by using Eqs. (3) and (2) that

$$\Delta Q = AkT\, N_{ss}(E_{max}) \quad , \tag{4}$$

where A is a constant and where $E_{max} = kT \ln (\sigma v_{th} N_c \tau)$. It has been assumed that $\sigma(E)$ and $N_{ss}(E)$ are relatively constant with respect to energies within kT of E_{max}. Since the density of states for a given sample is fixed, the capture cross-section can be shown to be[22]

$$1/\sigma_n = \tau v_{th} N_c \left(\frac{\tau}{\tau'}\right)^{-T'/(T-T')} \quad , \tag{5}$$

where τ, τ' are time constants corresponding to temperatures T, T' for a fixed interface state density $N_{ss}(E) \propto \Delta Q/kT$. This value is an average between temperatures T and T'.

Thus, the procedure for obtaining an interface state spectrum is 1) to measure ΔQ vs T for separate time constants τ, 2) calculate σ vs T from these data by using Eq. (5), and 3) calculate the relation between E_{max} and T by using the form of $\sigma(T)$ obtained in the last part of the procedure. It should be pointed out that the resulting density of states obtained is relatively insensitive to $\sigma(T)$ since this function enters logarithmically.

4.3 FET Development

Fabrication of field effect transistors will be investigated in order to determine the operating properties of actual MIS devices using the AlN/GaAs materials system. Such fabrication would be the first step in development of a viable GaAs MIS technology. We will need to develop a simple process involving a minimal number of steps for making FETs. To minimize cost and time delays, we will attempt to use existing masks for GaAs MESFETs. An

example of an anticipated process is shown in Fig. 10. This process is compatible with the existing processing available routinely at the Rockwell International facility in Thousand Oaks. The process requires three mask steps to make a self-aligned gate AlN/GaAs MISFET. Processing steps which require additional investigation in this program to make an FET involve activation of the Se implant, development of gate metallization which is stable upon annealing, and etching procedures to open holes for ohmic contacts to the GaAs.

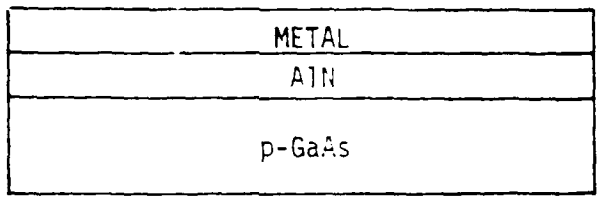
4.3.1 Implant Activation

One of the important advantages of using AlN as a dielectric for GaAs MIS devices is that the material has been demonstrated to be an excellent cap material for GaAs anneals subsequent to ion implantation. To make a FET with the process we have described, it will be necessary to use ion implantation to form drain and source regions of the FET and to anneal out implantation-related damage in the GaAs. This will require integrity of the AlN produced by our process through the implant and anneal procedures.

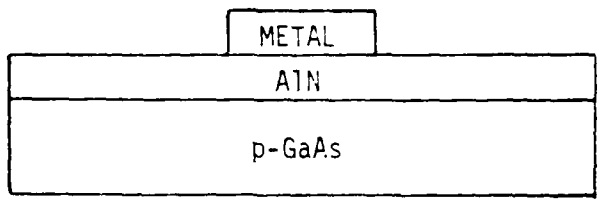
4.3.2 Gate Metalization

It will probably be necessary to cap the AlN with a metal subsequent to growth within the MBE growth chamber to prevent oxidation under the gate region. Such oxidiation, as discussed in Section 3.2.3, may cause hysteresis in the electrical properties of the MIS structure. Since the device must undergo subsequent anneal cycles following implantation to form a device, the metalization should be stable to 800°C; Al melts below this temperature. A number of possible substitutes exist which might be acceptable and which are compatible with our deposition system. These include Ti, reactively evaporated TiN, W, and a number of refractory metals which can be deposited by using a novel electron bombardment evaporator[23] as a source.

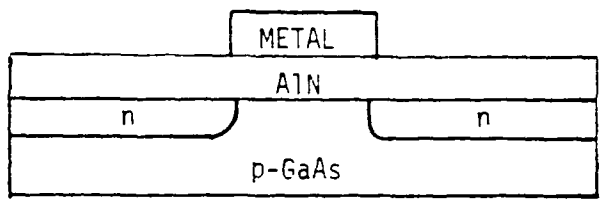
1. FILM GROWTH



2. GATE DEFINITION
   a. Photolithography
   b. Etch



3. Se IMPLANT
   a. Photolithography
   b. Implant
   c. Strip
   d. Anneal



4. OHMIC DEFINITION
   a. Photolithography
   b. Etch
   c. Evaporation
   d. Lift-Off
   e. Alloy

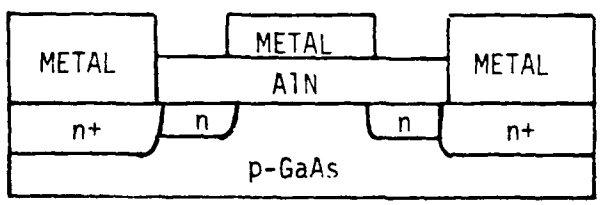


Fig. 10 Schematic of possible process to fabricate GaAs MISFET.

4.3.3 AlN Processing

We will study the effects on the AlN layers of various processing steps used to pattern the AlN. A number of wet chemical processes are available for etching AlN. Warm potassium hydroxide, for example, etches AlN quite easily. Hydrofluoric acid etches AlN, but the etch rate is slow, typically < 100Å/min. We may find that mobile ions introduced during such processing will have an adverse effect on device properties. In this case, we will investigate dry etching procedures such as reactive ion etching and ion milling of AlN/GaAs structures. Chlorine based plasma etching procedures would seem to be promising candidates for etching AlN, since this type of procedure attacks Al easily and is used routinely in the Si industry for patterning Al.

4.4 Additional Studies

In this section we propose studies of MIS characteristics of AlN interfaces formed on selected III-V semiconductors and investigation of the possibility of doping AlN with shallow donors.

4.4.1 Other Materials

MIS devices which involve III-V compounds other than GaAs are also of great technical interest. InP has good high field carrier saturation characteristics. InAs and $Ga_xIn_{1-x}As$ alloys have higher low field mobilities and better high field properties than GaAs. In addition, intrinsic surface state concentrations may be lower for these material systems than for GaAs. It should be pointed out that MESFET devices are not practical in the above material systems because they have low Schottky barrier heights.

The arguments we have previously developed in Section 2 for utilizing AlN as an insulator on GaAs are essentially the same for using AlN on any III-V semiconductor. AlN films will be deposited onto InP, InAs and selected alloy systems such as $Ga_xIn_{1-x}As$ and MIS properties of these interfaces will be determined.

4.4.2 Doping Studies

Because AlN has a bandgap of 6 eV as compared to 1.43 eV for GaAs, we expect that a considerable energy discontinuity exists between the conduction and valence band edges of the two materials; this band offset will be measured as mentioned in Section 4.1.1. It may be possible to use these offsets for the purposes of developing special devices. If the AlN/GaAs system is viewed as a heterojunction rather than as an insulator-semiconductor system, it becomes clear that analogies can be made with the AlAs/GaAs system. Because the AlAs/GaAs system has a low density of interface states, it is possible to get carrier transfer from the large bandgap material, AlAs, to the GaAs. Such effects have been exploited to produce high electron mobility FETs.

The principle difference between using AlN and AlAs in a heterostructure is that AlN has a much larger bandgap (6 eV compared to 2.2 eV). Consequently, impurity and defect states in the AlN can change the surface potential of GaAs through the same type of carrier transfer which occurs for the AlAs/GaAs system. If it is possible to dope AlN with donor impurities such as S or Se, it should be possible to obtain high mobility conduction in the GaAs without intentional doping of the GaAs. As with AlAs/GaAs structures, this carrier transfer could be exploited to obtain high mobility devices. Such effects will be investigated by implanting AlN/GaAs layers with various dopants to determine whether carrier transfer occurs.

5.0 WORK STATEMENT

First Year

1. Investigate possible reduction of AlN/GaAs interface states by thermally cleaning substrates in arsenic flux.
2. Determine importance of residual oxygen contamination on bulk and interface AlN/GaAs MIS properties.
3. Characterize AlN/GaAs MIS structures with different crystallographic orientations and with substrate material from different sources.
4. Develop AlN processing capabilities.
5. Fabricate and test simple FET structure from material with most promising MIS results.
6. Evaluate progress to decide if second year of program should be initiated.

Second Year

1. Refine most important processing parameters to optimize MIS structure.
2. Continue analysis of FET measurements.
3. Fabricate and analyze refined FET device structure(s).
4. Investigate possibility of doping AlN with shallow donors for transfered electron applications in GaAs.
5. Characterize MIS properties of AlN on other III-V semiconductors (e.g., InP, InAs, and selected alloys).

6.0 FACILITIES

Rockwell International consists of a number of operations and groups, each of which comprises several operating divisions. Each operating division functions independently with responsibility for its own programs in its area of technical capability. In addition, each division can call on the full complement of corporate resources to support a program. Company policy encourages the interchange of technical skills and physical support.

Rockwell International Microelectronics Research and Development Center (MRDC) conducts a comprehensive electronics research program on selected technologies and their applications in support of the electronics operations of Rockwell International. It performs the dual roles of exploring advanced concepts, devices, and technologies of future interest to electronics operations and of supporting their current technological commitments. The MRDC is located in facilities in Anaheim and Thousand Oaks, California. It operates under the direction of E. E. Pentecost, Vice President.

The Anaheim facility emphasizes silicon device technology while the Thousand Oaks, facility has a number of programs for the development of advanced semiconductor devices fabricated from GaAs and other III-V alloy compounds. These programs include development of digital and monolithic integrated circuits, high electron mobility transistors, heterojunction bipolar transistors, charge coupled devices, avalanche photodiodes, and semiconductor lasers.

Compound semiconductor device research has increased substantially during the past years. As efforts to improve device performance expand, the electronic properties of several compound semiconductors become of increasing importance. These properties motivate the use of compound semiconductors in place of silicon for many state-of-the-art, high performance, solid-state devices. Progress toward development of compound semiconductor devices which have performance characteristics corresponding to design expectations is frequently limited by insufficient understanding of the factors that influence interface properties. Expanded knowledge of these factors will directly aid device development programs.

Several interface characterization techniques exist at the Rockwell International Thousand Oaks Facility. A tool of major importance for any surface or interface characterization study is XPS. The Rockwell International Thousand Oaks Facility has the Hewlett-Packard 5950A XPS spectrometer with a unique ultrahigh vacuum (base pressure $<10^{-10}$ torr) sample preparation chamber modification. The preparation chamber contains a low energy electron diffraction (LEED) apparatus, a rastered ion sputter gun, several general purpose thin film evaporators and a residual gas analyzer. Several Auger spectrometers are in operation and a scanning Auger microscope (PHI model 590) with submicron spatial resolution is available. Two SEMS are located at the Rockwell International Thousand Oaks, Facility in addition to extensive optical microscopy equipment (which includes a Zeiss Ultraphot II).

DLTS measurements can be routinely carried out. An Air Products Helitran system is used to change the temperature of a sample. Capacitance transients are measured with a PAR 410 C-V plotter Transients are stored and averaged in a MACSYM computer which is also used for subsequent data analysis. It is also possible to use this system for measuring current transients or for exciting the sample with a wavelength tunable light source. In addition analytical techniques for current vs voltage, conductance vs voltage, capacitance vs voltage, Hall effect, photoluminescence, optical transmission and reflectivity, x-ray diffraction, electron microscopy, and ac admittance measurements are all available.

Three MBE systems are currently in use at Rockwell International in Thousand Oaks. These systems are used to prepare GaAs, AlAs, InAs, GaSb and several alloys. The bulk crystal growth facility includes a Melbourn high pressure Liquid Encapsulated Czochralski growth system for pulling high purity, large diameter GaAs crystals. Equipment for slicing and polishing wafers is also located in MRDC. Bulk Bridgman grown GaAs, InP, and InAs materials would be purchased from outside vendors.

Extensive facilities for device fabrication exist within MRDC including a full array of equipment required for GaAs processing. The processing

facilities are housed in a specially constructed complex of 5 interconnecting class - 100 laboratories designed to provide the ultra clean environment necessary for fabrication of high density devices with micron geometries. Included in this laboratory complex are the optical lithography facilities, chemical hoods, three vacuum systems for metals evaporation with two beam multiple hearth sources and one electron assisted filament source, a magnetron sputtering system, three sputtering systems for dielectrics, systems for plasma deposition and etching, an ion milling facility, alloy and annealing furnaces and diagnostic tools such as high precision metallurgical microscopes, a wafer probe station, a profilometer and ellipsometer.

Dielectric encapsulation systems for Si_3N_4 and SiO_2 are located in this clean room complex. A full spectrum of deposition techniques and appropriate masking technologies for these materials are available. The precise etching of fine line geometries in materials such as Si_3N_4 and SiO_2 is accomplished by plasma etching techniques. Plasma etching equipment includes both the traditional inductively coupled tunnel reactor and the more newly developed reactive ion etching (RIE) reactor. In addition, an ion milling system has been installed for a fine line etching capability.

The Rockwell International MRDC is equipped with three ion implantation systems, used in a variety of research and development applications. The 400 keV Varian Extrion ion implantation system is equipped with a cold cathode source and optional boiler oven, for providing a wide variety of ion species at high energy. The system utilizes a microprocessor for precise dose measurement, and cryopumps for minimizing surface contamination. The Extrion system can accommodate three-inch round substrates, as well as irregular sample sizes. A second 200 keV ion implantation system utilizes a hot filament source to provide high beam currents of species such as beryllium, as well as other metals. A third ion implantation system, based on a Van de Graf accelerator, is capable of providing beams up to 500 keV, and is used primarily for proton bombardment or experimental applications. This system also has backscatering capability for thin solid films.